Notice of Allowability	Application No.	Applicant(s)	
	10/642,654	MIYAZAWA ET AL.	
	Examiner	Art Unit	
	Lucy P. Chien	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *application filed on 8/19/2003*.

2. ☒ The allowed claim(s) is/are *1,2,5,6*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *09715105* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Amended Title: Liquid crystal display device with variations of positions of peaks of depth distributions of concentration of impurities in polycrystalline being within 10% of thickness.

The following is an examiner's statement of reasons for allowance:

Claims 1,2,5,6, are allowed.

Regarding Claim 1

Yamazaki et al (US 5933205) discloses provided with a pixel area on a substrate having a plurality of gate lines (see figure 10 and other), a plurality of drain lines 350, a plurality of thin film transistors (shown at the intersection and elsewhere land a plurality of pixel electrodes P20 (shown in figures 13-14 and elsewhere) corresponding to said plurality of thin film transistors, and a drive circuit area disposed at a periphery of said substrate and having a drive circuit 352 and 364 (described at the bottom of column 10 and elsewhere) for driving said plurality of thin film transistors, said plurality of thin film transistors comprising: polycrystalline silicon semiconductor layer 13 crystallized by laser annealing (Column 5, rows 23-25) and the concentration of impurities introduced into the polycrystalline silicon semiconductor layer by implantation (Column 6, rows 25-

32) formed on said substrate 50, on said polycrystalline silicon semiconductor layer with a gate insulating film (shown in figures 14b and 14c) interposed therebetween, an insulating film 65 to cover said polycrystalline silicon semiconductor layer, said gate insulating film and said gate a polycrystalline a gate electrode 9 formed electrode, a drain electrode 72 formed on said insulating film and electrically connected to said polycrystalline silicon semiconductor layer, and a source electrode 71 formed on said insulating film, spaced from said drain electrode and electrically connected to said polycrystalline silicon semiconductor layer.

However the reference lacks the unevenness of a surface of said polycrystalline silicon semiconductor layer being within 10% of a thickness of said polycrystalline silicon semiconductor layer, and variations of positions of peaks of depth distributions of concentration of impurities introduced into said polycrystalline silicon semiconductor layer to determine a conductivity type thereof being within 10% of said thickness of said polycrystalline silicon semiconductor layer, said positions of said peaks being with respect to a surface of said substrate.

Claim 2 is dependent upon Claim 1, therefore is allowable.

Regarding Claim 5,

Yamazaki et al (US 5933205) discloses a liquid crystal display device provided with a pixel area on a substrate having a plurality of gate lines (see figure 10 and other), a plurality of drain lines 350, a plurality of thin film transistors (shown at the intersection and elsewhere land a plurality of pixel electrodes P20 (shown in figures 13-14 and elsewhere) corresponding to said plurality of thin film transistors, and a drive circuit area disposed at a periphery of said substrate and having a drive circuit 352 and 364

(described at the bottom of column 10 and elsewhere) for driving said plurality of thin film transistors, said plurality of thin film transistors comprising: a polycrystalline silicon semiconductor layer 13 formed on said substrate 50, a gate electrode 9 formed on said polycrystalline silicon semiconductor layer with a gate insulating 5Im (shown in figures 14b and 14c) interposed there between, an insulating film 65 to cover said polycrystalline silicon semiconductor layer, said gate insulating film and said gate electrode, a drain electrode 72 formed on said insulating film and electrically connected to said polycrystalline silicon semiconductor layer, from said drain electrode and electrically connected to said polycrystalline silicon semiconductor layer. and a source electrode 71 formed on said insulating film, spaced

However, the reference lacks variations of positions of peaks of depth distributions of concentration of impurities introduced into said polycrystalline silicon semiconductor layer to determine a conductivity type thereof being within 10% of said thickness of said polycrystalline silicon semiconductor layer, said positions of said peaks being with respect to a surface of said substrate.

Hsu (US 5932913) discloses (Column 7, rows 20-38) the distribution of doping impurities in the polycrystalline silicon. Hsu does not directly state variations of positions of peaks of depth distributions of concentration of impurities introduced into said polycrystalline silicon semiconductor layer to determine a conductivity type thereof being within 10% of said thickness of said polycrystalline silicon semiconductor layer, said positions of said peaks being with respect to a surface of said substrate.

Claim 6 is dependent upon Claim 5, therefore is allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucy P. Chien whose telephone number is 571-272-8579. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lucy P Chien

Examiner

Art Unit 2871

ANDREW SCHECHTER
PRIMARY EXAMINER